SAYAM SETHI

Email | Google Scholar | GitHub | LinkedIn

EDUCATION

PhD in Electrical and Computer Engineering August 2023 – 2028 (tentative)
Advisor: Dr. Jonathan Baker; The University of Texas at Austin *Austin, Texas*
GPA: **3.95/4**

Bachelor of Technology | **Dept. of Computer Science and Engineering** July 2019 – May 2023
Indian Institute of Technology, Delhi *Delhi, India*
GPA: **9.55/10**

RESEARCH DIRECTION

I am interested in working on Quantum Error Correcting (QEC) architectures, specifically the compilation aspect for different error-correcting codes such as surface codes, qLDPC etc. I have been looking at the largely unexplored domain of dynamic compilation which involve making circuit execution decisions based on measurement results and/or Repeat-Until-Success (RUS) protocols. I also plan to explore problems related to minimising resource consumption and utilisation, for both classical post-processing overheads such as decoders, and quantum resources such as number of ancillas, distillation factories etc.

PUBLICATIONS

RESCQ: Realtime Scheduling for Continuous Angle QEC Architectures S. Sethi, and J. Baker
30th ACM International Conference on Architectural Support for Programming Languages and OS

- Worked with a non-traditional quantum surface code architecture that uses small angle rotation gates instead of magic state distillation
- Implemented a just-in-time compilation and scheduling strategy that uses ancilla qubits in the local neighbourhood to execute different gates
- Achieved 2x improvement in execution time compared to the baseline compilation and scheduling strategies

Cyclic Qubit Mappings M. Poster, S. Sethi, and J. Baker
2024 IEEE International Conference on Quantum Computing and Engineering (QCE)

- Investigated effects of variable error rates in a surface code grid on the program fidelity.
- Proposed a solution to achieve the average case error rate irrespective of the error distribution by cyclically mapping the data qubits over different paths of ancilla qubits.

Optimizing 3D DRAM Performance under Power and Thermal Constraints Jan 2022 – May 2023
IEEE TCAD Volume: 43 Issue: 8 *Undergraduate Thesis*

Memory Level:

- Studied the memory access patterns and their affect on the temperature of the HBM2E 3D Memory for multiple SPEC and PARSEC workloads
- Leveraged the thermal correlation between the vertically adjacent ranks with a reward-based power allocation policy **3D-TemPo** to simultaneously perform Dynamic Thermal Management
- Benchmarked with multiple baseline integrated policies such as round-robin, MFU, etc and existing DTM policies to achieve an execution time speedup of upto 17.94 times

System Level: *(extension to the publication)*

- Extended the 3D-TemPo work to incorporate power budgeting at the system level, for both memory and cores using a modified reward function
- Greatly reduced the energy consumption and execution times by using an average of 20% lesser energy and 15% lesser time than the baseline implementation

Internships

IBM Research, TJ Watson Research Center May – Aug 2024

Quantum Research Scientist Intern

- Systematically explored the space of **Explainable AI** in the context of **Quantum Machine Learning** to understand and compare the learning process of quantum models versus classical models
- Designed a framework to compute Shapley values for an arbitrary black-box model that involves projected quantum feature maps such as Heisenberg ansatz, Pauli feature maps, etc
- Observed significantly lower correlations (upto a drop of 0.5) in the explanations given by models using quantum ansatz as compared to the explanations given by purely classical models

Quadeye Securities LLP, Gurugram Jun – Jul 2022

Systems Intern

- Developed an HTTP/2 Client library along with a parser to encode and decode HTTP/2 frames
- Designed data structures to reduce latency of features like stream lifecycle, HPACK and Huffman encoding
- Enhanced security by adding TLS support, extensively tested library using unit tests and stress testing
- Performed optimisations to reduce i-cache misses and memory allocation to get an average parse time of 300ns

Academic Achievements

- **IIT Delhi Semester Merit Award**: Secured for being in the **top 7 percentile** in **Semester I** of **2019-20** and **2021-22**
- **ICPC India Regionals, Amritapuri '21**: Secured **India Rank 47** and **Institute Rank 1** out of **4393 teams**
- **Google HashCode '22**: Secured **India Rank 12**, **Institute Rank 1** and **Global Rank 240** out of **10177 teams**
- **Indian National Mathematical Olympiad**: Qualified for **INMO 2018** (precursor to IMO) on being shortlisted in the Telangana region in **RMO 2017**
- **Kishore Vaigyanik Protsahan Yojana (KVPY)**: Offered the fellowship in **SX stream (2018-19)** and **SA stream (2017-18)** with **All India Ranks** of **34** and **271** respectively

Technical Skills

Programming Languages: C, C++, Python, Java, VHDL, Assembly, Standard ML, Octave, MATLAB, R
Libraries/Frameworks and Tools: Qiskit, Stim, Sniper, HotSpot, CoMeT, Vivado, LaTeX, git

Relevant Coursework

UT Austin: Quantum Systems from a Software and Arch Perspective, Parallel Computer Architecture, Topics in Quantum Computing : Quantum Error Correction, Quantum Information and Computing, Quantum Complexity Theory, Unconventional Computation

IIT Delhi: Quantum and Post Quantum Cryptography, Synthesis of Digital Systems, Architecture of High Performance Computers, Advanced Topics in Embedded Computing, Special Topics in Hardware Systems, Digital Logic and System Design, Computer Architecture, Compiler Design, Cryptography and Computer Security, Operating Systems, Analysis and Design of Algorithms, Principles of Artificial Intelligence, Machine Learning, Probability and Stochastic Processes, Linear Algebra, Differential Equations, Calculus

Extra-Curricular Activities

Teaching Assistant

- Grad TA for ECE 312 - Software Design & Implementation in Fall '24, Spring '25, course for ECE sophomores
- Grad TA for ECE 306 - Introduction to Computing in Fall '23, introductory course for ECE freshers
- Head TA for COL216 - Computer Architecture in Spring '23, core course for CSE sophomores
- TA for COL215 - Digital Logic and System Design in Fall '22, core course for CSE sophomores

Algorithms and Coding Club, IIT Delhi

- **Overall Coordinator, 2022-23**: Got the club promoted from a Chapter to a Technical Club; organized events in Tryst, Technical Fest at IITD
- **Coordinator, 2021-22**: Conducted the Summer of CP and took live lectures on YouTube; guided executives
- **Executive, 2020-21**: Authored various problems for Competitive Programming contests conducted by the club